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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,557	11/06/2003	Hiroshi Yamamoto	8038-1049	9561

466 7590 08/23/2005

YOUNG & THOMPSON
745 SOUTH 23RD STREET
2ND FLOOR
ARLINGTON, VA 22202

EXAMINER	
NGUYEN, HIEP	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/701,557	YAMAMOTO, HIROSHI	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *attached paper*.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Elassaad et al. (US 2004/0257207A1) in view of Porterfield (US Pat. 6,588,001) and Kumamoto (US Pat. 4,695,748).

Regarding claim 3, figure 3 of Elassaad shows a semiconductor device comprising: a plurality of repeaters (Sopt), inserted in the transmission line to divide the signal transmission line into a plurality of divided signal lines. Figure 3 of Elassaad does not show that each repeater comprises two inverters and the first inverter is larger than the second inverter. However, it is old and well known to an artisan having skilled in the art that a buffer comprises two inverters and it can be used as repeater (see Porterfield, US Pat. 6,588,001; Fig. 2, col.1, lines 55-67). Figure 2 of Porterfield does not show that the first inverter (220) is larger than the second inverter (215). Figure 1 of Kumamoto teaches a repeater circuit comprising two inverters (6) and (9) where in, the first inverter (6) is larger than the second inverter (9) for providing a repeater that can detect the input voltage precisely at high speed (Abstract). Therefore, it would have been obvious to an artisan having skills in the art to replace the repeater of Porterfield with the repeater taught by Kumamoto for providing a repeater that can detect an input voltage precisely at high speed.

Regarding claim 4, it is inherent that the divided signal lines, the distances between the repeaters are longer than the distance between two inverters that form the repeater.

Regarding claims 5 and 6, the combination of Elassaad, Porterfield and Kumamoto shows a branch comprising another repeater (B, see attached paper) that includes a repeater, taught by Kumamoto, including two inverters; the first inverter having a current driveability

larger than a current driveability of said second inverter. The input signal applied to the first inverter (A) is a clock signal.

Regarding claim 7, figures 3 and 6 of Elassaad show that the signal line has wire capacitance (Cw). The wire capacitance causes wire delay that is at least 7 times that of the driver (paragraph [0112]). Thus, the signal line has a higher capacitance than an input capacitance of the repeater.

Regarding claim 8, figures 3 and 6 of Elassaad show a semiconductor device comprising: first and second functional blocks, not shown, connected via a signal transmission line; plurality of repeaters (A, B) in the transmission line that divide the signal transmission line into plural divided signal lines, each of the divided signal lines having a higher capacitance than an input capacitance of a respective one of said repeaters connected thereto (paragraph [0112]). Figure 3 of Elassaad does not show that each repeater comprises two inverters and the first inverter is larger than the second inverter. However, it is old and well known to an artisan having skilled in the art that a buffer comprises two inverters and it can be used as repeater (see Porterfield, US Pat. 6,588,001; Fig. 2; col. 1, lines 55-67). Figure 2 of Porterfield does not show that the first inverter (220) is larger than the second inverter (215). Figure 1 of Kumamoto teaches a repeater circuit comprising two inverters (6) and (9) where in, the first inverter (6) is larger than the second inverter (9) for providing a repeater that can detect an input voltage precisely at high speed (Abstract). Therefore, it would have been obvious to an artisan having skills in the art to replace the repeater of Porterfield with the repeater taught by Kumamoto for providing a repeater that can detect an input voltage precisely at high speed.

Conclusion

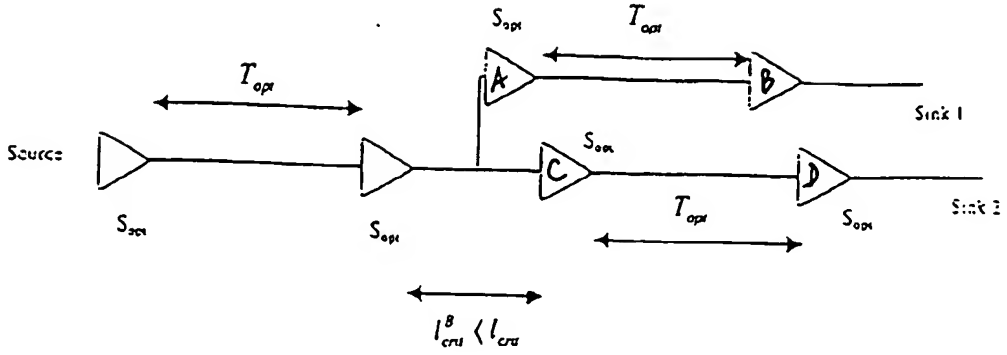
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
08-18-05

TUAN T. LAM
PRIMARY EXAMINER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$l^{B}_{crit} < l_{crit}$

Fig. 3

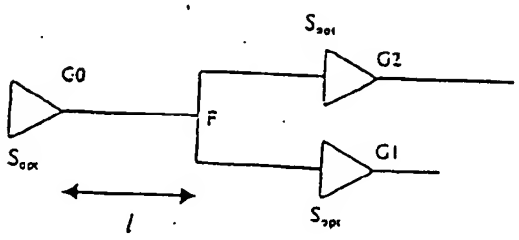
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Fig. 4